

Structure of Metal Oxide Semiconductor Field Effect Transistor

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Field of the invention

The present invention relates to MOSFET (Metal Oxide Semiconductor Field Effect Transistor) for modifying Schottky Barrier and diminishing Carrier Injection Resistance. More particularly, the present invention employs SOI (Silicon-On-Insulator) device to be a substrate thereof for modifying Schottky Barrier and diminishing Carrier Injection Resistance, and a fabrication process therefor.

Background of the invention

The MOSFET industry has been working on downscaling for microelectronic devices, particularly for the MOSFET, to increase its features

and the density of component. It is very successful in some examples from the early micron till today's deep-submicron for MOSFET, however, it still has some problems for downscaling to nanomicon. Especially, the short channel effect is a very important problem, which is caused by crosswise dopant diffusion; after ion implanting in source and drain electrodes, annealing process may cause the crosswise dopant diffusion.

Lately, the structure of Schottky Barrier has been put in use on nanomicon SOI device. Metal silicide may replace the P-N junction without causing dopant diffusion; therefore, it may solve the problem of short channel effect. The structure of Schottky Barrier has been provided in 10 years ago for improving the latch-up problem, but it also caused high carriers injection resistance in source electrode and high current leakage in drain electrode of Schottky Barrier. Though an asymmetric structure has been provided for solving the problem of current leakage, it could not be accepted by CMOS process due to the different mask process for masking the source region, and the resistance problem still not be solved.

The structure of Schottky Barrier being employed on SOI device may improve the current leakage in drain electrode. Because after forming metal silicide the silicon layer is reacted completely, the area of Schottky Junction is

squeezed in the channel for carriers passing through, and the current leakage problem may be improved dramatically. However, the problem of carrier injection resistance is still not solved. Besides, due to the different density channel of N-MOSFET and P-MOSFET respectively, it is necessary to have different metal-silicide for modifying Schottky Barrier, for example, PtSi adapted for P-MOSFET and ErSi₂ for N-MOSFET. Therefore, it may not be available for integrating into the standard MOS process with different materials.

Furthermore, "Sub-gate" has been provided to form "inversion layer" for generating a channel for carriers passing through; however, this kind of process is not accepted for the standard CMOS process, and also, the problem of employing different material is not solved. In addition, it needs high voltage to control the sub-gate, and it also may cause another problem in voltage control.

Summery of the invention

Accordingly, the present invention discloses a structure of MOSFET for modifying the Schottky Barrier and diminishing carrier Injection Resistance and method for fabricating the same, which comprises a SOI (Silicon-On-

Insulator) device, a MOS (Metal Oxide Semiconductor) formed on said SOI device, and a metal-silicide layer. Said SOI device includes a substrate, an insulation layer formed on said substrate, and a silicon layer formed on said insulation layer. Said MOS is formed on said SOI device. The metal-silicide layer is formed in accordance with a metal self aligned process by a metal layer being deposited on said SOI device and on said MOS for reacting with said silicon layer, and an implant-to-silicide process is employed to form a high-density source region and a high-density drain region for modifying Schottky Barrier and diminishing Carrier Injection Resistance.

Brief description of the drawings

The present invention will be better understood from the following detailed description of preferred embodiments of the invention, taken in conjunction with the accompanying drawings, in which

FIG. 1 is a schematic cross section of a SOI device;

FIG. 2 is a schematic cross section of a MOS formed on the SOI device; and

FIG. 3 ~ FIG. 7 are schematic cross sections of the essential portion illustrating a process for manufacturing the MOSFET according to the

present invention.

Description of the preferred embodiments

The following descriptions of the preferred embodiments are provided to understand the features and the structures of the present invention.

Please referring to the FIG. 1 of a schematic cross section of a SOI device, it shows a SOI device 1 formed by a SOI process to be the substrate of the present invention. The SOI device 1 includes a substrate 11, an insulation layer 12 formed on said substrate 11, and a silicon layer 13 formed on said insulation layer 12; wherein said substrate 11 may be a silicon substrate or a glass substrate, and said insulation layer 12 may be an oxide layer. Next, please seeing the FIG. 2, the isolation area 14 is formed by a general isolation process. Then the process of dielectric oxidization or deposition, gate deposition, photolithography, and etching forms the gate isolation layer 22 and gate electrode 21. After that, depositing a dielectric isolation layer and adapting an anisotropic etching process, the spacers 23 will be formed. Thus, a MOS 2 is formed on said SOI device 1; wherein said MOS is selected from one of a P-MOS or an N-MOS.

Next, after depositing a metal layer 31, referring to the FIG. 3 ~ FIG. 5,

the silicon layer 13 may be reacted by the metal self-aligned silicide process to form a metal-silicide layer 3, and thereby, adapting an implant-to-silicide and annealing process, after forming said metal-silicide layer 3 further comprises the step of annealing process, which is processed after the implant-to-silicide for implanting carriers into said silicide layer processing, a high-density source region and a high-density drain region 24 and 25, as shown in the FIG. 7, are formed for modifying Schottky Barrier and diminishing Carriers Injection Resistance; wherein said MOS 2 further comprises a channel between source electrode and drain electrode for carriers passing through. Because the high-density source and drain regions 24 and 25 forms the modified Schottky Junction, which can solve dramatically the problem of leakage current. Furthermore, the source and the drain regions are completely reacted in metal silicide, therefore, the sheet resistance may be limited. In addition, the present invention adapts the ion-implantation to get the feature of metal silicide, and therefore, the process temperature won't be high, only about 600°C. It is another object of the present invention to provide a low temperature process.

Or, before the self-aligned silicide process in accordance with this invention, the ion implantation will be processed (implant-to-metal) with

proper dopant, and then, a high-density source region and a high-density drain region will be formed. That is, referring to the FIG. 1 ~ FIG. 3, a SOI device 1 formed by a SOI process to be the substrate of the present invention. The SOI device 1 includes a substrate 11, an insulation layer 12 formed on said substrate 11, and a silicon layer 13 formed on said insulation layer 12; wherein said substrate 11 may be a silicon substrate or a glass substrate, and said insulation layer 12 may be an oxide layer. Next, please seeing the FIG. 2, the isolation area 14 is formed by a general isolation process. Then the process of dielectric oxidization or deposition, gate deposition, photolithography, and etching forms the gate isolation layer 22 and gate electrode 21. After that, depositing a dielectric isolation layer and adapting an anisotropic etching process, the spacers 23 will be formed. Thus, a MOS 2 is formed on said SOI device 1; wherein said MOS is selected from one of a P-MOS or an N-MOS. After depositing the metal layer 31, then referring to the FIG. 6 and FIG. 7, the ion implantation is processed (implant-to-metal) with proper dopant to form a metal-silicide layer 30 by said metal layer 31 reacting with said silicon layer 13 in accordance with the metal self-aligned process. Therefore, a high-density source region 24 and a high-density drain region 25 are formed for

modifying the Schottky Barrier and diminishing Carrier Injection Resistance, as shown in the FIG. 7; wherein said MOS 2 further comprises a channel between source electrode and drain electrode for carriers passing through. Because the high-density source and drain regions 24 and 25 forms the modified Schottky Junction, which can solve the problem of leakage current in drain electrode. Furthermore, the source and the drain are completely reacted in metal silicide, therefore, the sheet resistance may be limited. In addition, the present invention adapts the ion-implantation to get the feature of metal silicide, and therefore, the process temperature won't be high, only about 600°C. It is another object of the present invention to provide a low temperature process.

The present invention may be embodied in other specific forms without departing from the spirit of the essential attributes thereof; therefore, the illustrated embodiment should be considered in all respects as illustrative and not restrictive, reference being made to the appended claims rather than to the foregoing description to indicate the scope of the invention.